REMARKS

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicants note that the Office Action indicates at page 6, paragraph 5, that claims 4-7, 10, 17, 21-24, 26 and 33 would be allowable if rewritten in independent form. Accordingly, new independent claims 34, 38-40 and 43-45 submitted herewith are allowable claims 4, 10, 17, 21, 24, 26 and 33, respectively, rewritten in independent form and are believed to be allowable. New dependent claims 35-37 depend from allowable claim 34, and new dependent claims 41 and 42 depend from allowable claim 40, and, therefore, are also believed to be allowable.

The disclosure is objected to because of informalities stated in the Office Action. The disclosure is amended above in a manner believed to overcome the objection. Therefore, reconsideration of the objection is requested.

Claims 1-3, 8-9, 11-16, 18-20, 25 and 27-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau, *et al.* (U.S. Patent Number 6,518,155). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-17, a method of fabricating a MOS transistor includes forming an insulated gate pattern on a semiconductor substrate and further forming spacers covering sidewalls of the gate pattern. Before forming the spacers, impurity ions are injected into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD of a first conductivity type and a halo of a second conductivity type.

Claims 1-17 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that, before forming the spacers, impurity ions are injected into the semiconductor substrate using the gate pattern as an ion injection mask to form an LDD of a first conductivity type and a halo of a second conductivity type. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 18-33, a method of fabricating a CMOS transistor includes defining an NMOS transistor region and a PMOS transistor region on a predetermined portion of a semiconductor substrate. Insulated gate patterns are formed on the NMOS and PMOS transistor regions and spacers are formed on the gate patterns. Before forming the spacers, impurity ions are injected into the NMOS and PMOS transistor regions on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs of a first conductivity type in the NMOS region and of a second conductivity type in the PMOS region and to form halos of the second conductivity type in the NMOS region and of the first conductivity type in the PMOS region.

Claims 18-33 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that, before forming the spacers, impurity ions are injected into the NMOS and PMOS transistor regions on the semiconductor substrate using the gate patterns as an ion injection mask to form LDDs of a first conductivity type in the NMOS region and of a second conductivity type in the PMOS region and to form halos of the second conductivity type in the NMOS region and of the first conductivity type in the PMOS region. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Chau, *et al.* discloses a method for reducing silicide encroachment including forming intermediate electrodes 324. After the intermediate electrodes 324 are formed, tip regions or lightly doped regions can be formed. For example, n-type conductivity tip regions 326 can be formed in p-type conductivity region 314 and p-type conductivity tip regions 328 may be formed in n-type conductivity region 316.

Chau, *et al.* fails to teach or suggest that, before forming spacers, impurity ions are injected into a semiconductor substrate using a gate pattern as an ion injection mask to form an LDD of a first conductivity type and a halo of a second conductivity type, as claimed in claims 1-17. Instead in Chau, et al., the tip regions or lightly doped regions are formed in the n-type or p-type region of a conductivity type different than the n-type or p-type region in which it is formed,

rather than forming an LDD of a first conductivity type and a halo of a second conductivity type, as claimed.

Further, Chau, *et al.* fails to teach or suggest that, before forming spacers, impurity ions are injected into NMOS and PMOS transistor regions on a semiconductor substrate using gate patterns as an ion injection mask to form LDDs of a first conductivity type in the NMOS region and of a second conductivity type in the PMOS region and to form halos of the second conductivity type in the NMOS region and of the first conductivity type in the PMOS region, as claimed in claims 18-33. Instead, in the n-type conductivity tip regions 326 are formed in the p-type conductivity region 314 and the p-type conductivity tip regions 328 are formed in the n-type conductivity region 316, thus failing to teach or suggest forming both an LDD and a halo of opposite conductivity types in an NMOS region and a PMOS region.

As discussed above, Chau, *et al.* fails to teach or suggest certain elements of the invention set forth in the claims. Specifically, Chau, *et al.* fails to teach or suggest that, before forming spacers, impurity ions are injected into a semiconductor substrate using a gate pattern as an ion injection mask to form an LDD of a first conductivity type and a halo of a second conductivity type, as claimed in claims 1-17. Further, Chau, *et al.* fails to teach or suggest that, before forming spacers, impurity ions are injected into NMOS and PMOS transistor regions on a semiconductor substrate using gate patterns as an ion injection mask to form LDDs of a first conductivity type in the NMOS region and of a second conductivity type in the PMOS region and to form halos of the second conductivity type in the NMOS region and of the first conductivity type in the PMOS region, as claimed in claims 18-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-3, 8-9, 11-16, 18-20, 25 and 27-32 under U.S.C. 102(e) as being anticipated by Chau, *et al.* is respectfully requested.

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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